REMARKS

This application has been carefully reviewed in light of the Office Action dated April 30, 2008. Claims 1-15 remain in this application. Claims 1 and 14 are the independent Claims. It is believed that no new matter is involved in the arguments presented herein.

Reconsideration is respectfully requested.

Art-Based Rejections

Claims 1, 3, and 8 were rejected under 35 U.S.C. § 103(a) over U.S. Patent No. 4,776,894 (Watanabe) in view of U.S. Patent No. 4,926,230 (Yamagishi); Claims 2 and 4-7 were rejected as Claim 1, and further in view of JP Pub. No.59-35016 (Nakamura); Claim 10 was rejected as Claim 1, and further in view of U.S. Patent No. 4,875,944 (Yoshida); Claims 11 – 13 as Claim 1, and further in view of JP Pub. No. 2002-170973 (Kondo); Claims 14-15 were rejected under 35 U.S.C. § 103(a) over EP 1,198,014 (Hayashi) in view of Watanabe and Yamagishi.

Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the arguments below.

The Watanabe Reference

Watanable is directed to a photovoltaic device having a plurality of unit photovoltaic cells layered in optical series. Each unit photovoltaic cell includes an optically active layer made of amorphous silicon and two impurity doped layers of opposite conductivity types arranged at opposite sides of the optically active layer. A first impurity doped layer of a first unit photovoltaic cell locates at the contact interface with a second unit photovoltaic cell and is made of a first amorphous silicon alloy of first conductivity type. A second impurity doped layer of the second photovoltaic cell locates at the contact interface and is made of a second amorphous silicon alloy (*Watanabe Abstract*).

The Yamagishi Reference

Yamagishi is directed to a photovoltaic device of amorphous or microcrystalline semiconductor having multi-junction. One or more layers having high concentration impurities is interposed between p-type conductive layer and n-type conductive layer. A tunnel junction is formed by the interposed layer to improve the photo-electric conversion rate (*Yamagishi Abstract*).

The Nakamura Reference

Nakamura is directed to the preparation of silicon layer by vacuum metallization of silicon, CVD, or plasma. The preparation includes a first stage of keeping the silicon layer at 480-600 degree C and converting the silicon to crystalline. The second stage includes heat-treating the silicon in a plasma atmosphere containing hydrogen or its isotope at approximately the crystallite formation temperature of silicon (*Nakamura machine translation of CONSTITUTION section*).

The Yoshida Reference

Yoshida is directed to an amorphous photoelectric converting device that remains efficient despite exposure to heat over long periods of time. The device is formed by placing one on top of the other a plurality of photovoltaic elements each including a thin film of p-i-n structure. The p-type layer and the n-type layer of adjacent elements are made of microcrystalline silicon so that good ohmic contact is established, and the p-type layer of microcrystalline silicon contains boron in an amount sufficient to neutralize the donor atoms diffused from the adjacent n-type layer when the device is left to stand at high temperatures for a long period of time. The amount of boron, however, is limited to such an extent that the boron atoms do not adversely affect the initial desired characteristics of the device (*Yoshida Abstract*).

The Kondo Reference

Kondo is directed to a method of forming a semiconductor device having a silicon and two or more p-i-n junctions. The process includes the step of putting the p-type layer or n-type layer exposed to the surface of the p-i-n junction in an oxygen atmosphere after forming a p-i-n junction (*Kondo machine translation, paragraph [0008]*).

The Hayashi Reference

Hayashi is directed to a photovoltaic module including a transparent substrate and hybrid-type photovoltaic cells arrayed on the substrate and connected in series to each other. The cells includes a back electrode facing the substrate, a transparent front electrode intervening between the substrate and the back electrode, a first photovoltaic layer between the front and back electrodes and comprising an amorphous semiconductor layer. A second photovoltaic layer is disposed between the first photovoltaic layer and the back electrode and is formed of a crystalline semiconductor layer. A conductive interlayer with a light-transmitting-and-reflecting property is disposed between the first and second photovoltaic layers and having a thickness in a range of 10 nm to 100 nm and a specific resistance in a range of 1×10^{-3} Ω·cm to 1×10^{-1} Ω·cm (*Hayasho paragraph 57*).

The Claims are Patentable Over the Cited References

The present application is generally directed to a stacked-layer type thin-film photoelectric conversion device having improved conversion efficiency.

As defined by independent Claim 1, a stacked-layer type photoelectric conversion device includes a plurality of photoelectric conversion units stacked on a substrate, each of which includes a one conductivity-type layer, a photoelectric conversion layer of substantially intrinsic semiconductor, and an opposite conductivity-

type layer in this order from a light incident side. At least one of the opposite conductivity-type layer in a front photoelectric conversion unit arranged relatively closer to the light incident side and the one conductivity-type layer in a back photoelectric conversion unit arranged adjacent to the front photoelectric conversion unit includes a silicon composite layer at least in a part thereof. The silicon composite layer has a thickness of more than 20 nm and less than 130 nm and an oxygen concentration of more than 25 atomic % and less than 60 atomic %, and includes silicon-rich phase parts in an amorphous alloy phase of silicon and oxygen.

The applied references fail to disclose or suggest the above features of the claims of the present invention. In particular, the applied references fails to disclose or suggest the opposite conductivity-type layer in a front photoelectric conversion unit or the one conductivity-type layer in a back photoelectric conversion unit including a silicon composite layer, and the silicon composite layer has "a thickness of more than 20 nm and less than 130 nm and an oxygen concentration of more than 25 atomic % and less than 60 atomic %, and includes silicon-rich phase parts in an amorphous alloy phase of silicon and oxygen" as recited in Claim 1.

The Action asserts Watanabe teaches the features the silicon composite layer having "an oxygen concentration of more than 25 atomic % and less than 60 atomic %, and includes silicon-rich phase parts in an amorphous alloy phase of silicon and oxygen." The Action cites Watanabe col. 4, lines 36-48 and col.8, lines 36-39 as disclosing this feature. Applicant respectfully notes the cited portions of Watanabe are directed at the one conductivity-type layer or the opposite conductivity-type layer, and not the silicon composite layer recited in Claim 1.

Watanabe teaches two embodiments. FIG. 1 of Watanabe illustrates the first embodiment having one conductivity-type layer **33** and opposite conductivity-type layer **42**; that embodiment does not teach a separate layer that can be reasonably construed as the silicon composite layer recited in the claims. On the other hand, FIGS. 10-12 of

Watanabe illustrate the second embodiment having intermediate layers in addition to the one conductivity-type layer and the opposite conductivity-type layer. (FIG. 10 of Watanabe illustrates one conductivity-type layer **63** and the opposite conductivity-type layer **42**; the one conductivity-type layer **63** includes an intermediate layer **64**; FIG. 11 of Watanabe illustrates one conductivity-type layer **33** and the opposite conductivity-type layer **72**; the opposite conductivity-type layer **72** includes an intermediate layer **74**; FIG. 12 of Watanabe illustrates both intermediate layers **64** and **74**.)

Watanabe col. 4, lines 36-48 is directed to layers **33** and **42** of the first embodiment, and col.8, lines 36-39 is directed to layer **42** of the first embodiment. Watanabe does not teach or even suggest the second embodiment having the silicon composite layer as recited in the claims. Since the first embodiment as illustrated by FIG. 1 of Watanabe does not even have an intermediate layer that can be fairly construed as the silicon composite, Watanabe cannot be said to teach or suggest the features of silicon composite layer as recited in Claim 1.

Moreover, Applicant respectfully submits the cited portions of Watanabe does not teach or suggest the features as asserted in the Action. Even when applied to the silicon composite layer, the cited portions of Watanabe still fail to teach or suggest the features of the silicon composite layer recited in the claims. For example, the Action asserts that the Watanabe col. 4, lines 36-39 teaches the silicon composite layer having "an oxygen concentration of more than 25 atomic % and less than 60 atomic %." Applicant respectfully submits that assertion is improper. Watanabe col. 4, lines 30-39 recites the follow:

> It is confirmed from data obtained by the measurements as shown in FIGS. 6-9 that the photovoltaic efficiency (η) of a photovoltaic device according to the present invention is superior to that of Comparison Example 1 or 2 as long as **the amount (x) of nitrogen or carbon** in the p-type impurity doped layer 42 is kept equal to each other even when it is varied. It is found that the amount of

> the elements (besides silicon), **such as nitrogen**, contained in the impurity doped layer 42 is preferably 3-30%, more preferably 5-20%. (*Emphasis in bold added by Applicant.*)

As seen above, the cited portion of Watanabe is directed at nitrogen or carbon, and not oxygen content as recited in the claims. Moreover, FIGS. 6-9 referenced in the citation are direct at Examples 1-4 of Watanabe. As listed in TABLE 2 of Watanabe, Examples 1 and 2 do not even contain any oxygen. Examples 3 and 4 include layer **42** of a-$Si_{0.9}N_{0.05}O_{0.05}$. However, FIGS 6-9 only compare photoelectric efficiency to x, which is nitrogen or carbon. FIGS 6-9 does not reveal any information relating to oxygen level of layer **42**, let alone the oxygen level recited in the claims.

Accordingly, even if the cited portions of Watanabe are applicable to the silicon composite layer (and they are not), Watanabe still fails to teach or suggest the features of the silicon composite layer recited in Claim 1.

Moreover, the silicon composite layer in the present invention is one layer that includes a matrix of an amorphous silicon oxide phase and silicon-rich phase parts dispersed in the matrix. Therefore, the combination of the intermediate layer and the neighboring layer at the contact interface in Watanabe does not correspond to the silicon composite layer in the present invention.

Furthermore, Watanabe intends to use a combination of layers each having a wide band gap in order to reduce light absorption at the contact interface. On the other hand, the present invention intends to obtain the reflection effect by using a silicon composite layer having a low refractive index. Furthermore, Watanabe discloses no data of the oxygen concentration.

Yamagichi is not seen to remedy the deficiencies of Watanabe. Moreover, the Action concedes Watanabe failed to teach or suggest the feature that the silicon composite layer has "a thickness of more than 20 nm and less than 130 nm," and

applies Yamagishi as a remedy thereof. Applicant respectfully submits that assertion is improper.

Based on the Action's construction, Yamagishi teaches a the silicon composite layer having thickness of 1 – 30 nm (*Yamagishi col. 2, lines 38-41*). (The Action's assertion that the thickness taught by Yamagishi is 7 – 70 nm is inaccurate. Yamagishi at col. 2, lines 28-29 teaches the p-type layer **3** or the n-type layer **2** is 7 – 70 nm in thickness. However, the p-type layer **3** or the n-type layer **2** does not correspond to the silicon composite layer recited in the claims. See Yamagishi FIGURE for references to layer **2** and **3**.)

However, an applied reference merely teaching an overlapping range recited in the claims, as Yamagishi does under the Action's construction, is insufficient to render the claims obviousness under 103(a). Claims of optimization range are patentable when Applicant shows the criticality of the range or unexpected result derived from the claimed range (*see MPEP 2144.05 Obviousness of Ranges, B. III. REBUTTAL OF PRIMA FACIE CASE OF OBVIOUSNESS*). Here, Applicant's specification discloses that the high reflectance at interface level improves the performance of the stacked photoelectric conversion device (*page 14, last line – page 15, lines 3*). Moreover, the silicon composite layer thickness affects reflectance, and the silicon composite layer having thickness of 20 – 130 nm provides optimum reflectance (*Applicant specification FIG. 11*).

In contrast, Yamagishi does not teach or suggest that high reflectance at the interface improves the performance of the device, nor the relationship between the thickness of the silicon composite layer and reflectance. In fact, Yamagishi teaches that "the thicker the high impurity concentration layer, the greater the light absorption loss becomes." (*Yamagishi col. 2, lines 36-37*). Yamagishi thus cannot be said to teach or suggest the range of silicon composite layer thickness recited in Claim 1.

In sum, Watanabe and Yamagishi even combined do not disclose or suggest all the features recited in Claim 1, and therefore, cannot render obvious that claim. Claim 1 is thus allowable over Watanabe and Yamagishi, and such allowance is respectfully requested.

The ancillary references are not seen to remedy the deficiencies of Watanabe and Yamagishi. Claim 14 recites similar features as Claim 1 discussed above, and is thus also allowable over the applied reference. Allowance of Claim 14 is respectfully requested.

The remaining claims depend directly or indirectly from Claims 1 and 14, and are therefore allowable at least for the same reasons as base Claims 1 and 14. The allowance of those claims is respectfully requested.

For example, with respect to claims 11 and 12, Kondo discloses that the p-layer or n-layer of the first conversion unit is exposed to the atmosphere an then the opposite conductivity-type layer is deposited. In the present invention, by contrast, the silicon composite layer is once exposed to the atmosphere at an intermediate state of deposition thereof.

Conclusion

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4721 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

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By: _____
Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

1999 Avenue of the Stars
Suite 1400
Los Angeles, CA 90067
Phone: (310) 785-4600
Fax: (310) 785-4601